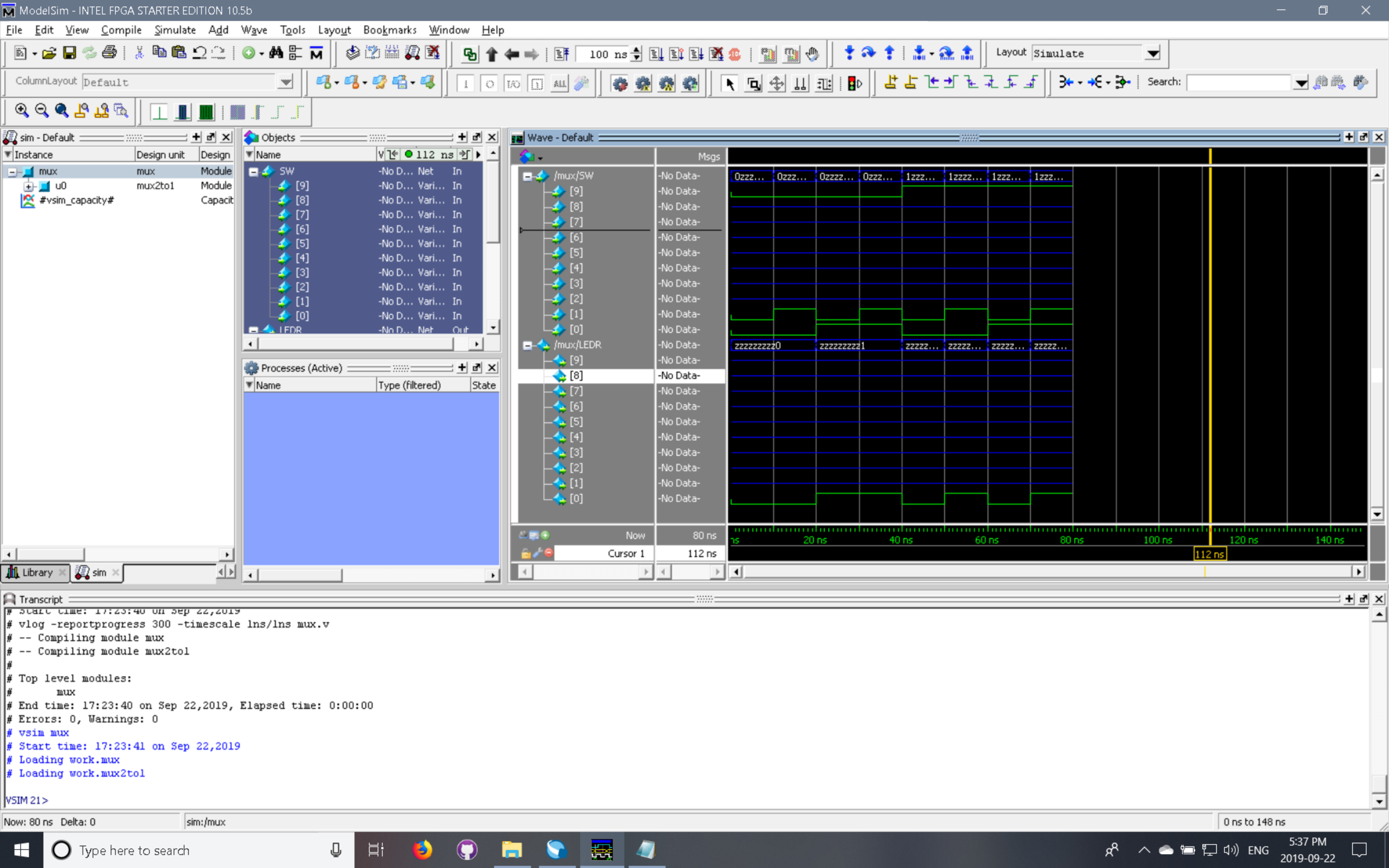
CSC258 LAB2 PRELAB

[TINGFENG XIA](https://tingfengx.github.io/), 1003780884, xiatingf

5 PART I

1. This is a screen shot of the output.



Our inputs are SW[0], SW[1], SW[9] and output is sent to LEDR[0], we ran each combination of input for 10ns. We have the output as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| SW[0] (x) | SW[1] (y) | SW[9] (s) | LEDR[0] (m) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

According to the results above, we can confirm that the design is working properly since when SW[9], i.e. input s, is zero, the output m is equal to SW[0] which is our x input and when SW[9] is 1, the output m is equal to the y input(SE[1]). So the multiplexer is correct.

6 PART II

1. Here we have 6 inputs in total to consider, so there would be rows in a full truth table.
2. Here is my design (Notice that I assumed the mux2to1 multiplexer to have the same input/output layout as specified in the handout.)

